

TC 4946

1030 USPTO  
12/94  
0/2001

314	Subclass	ISSUE CLASSIFICATION
257	Class	

## U.S. UTILITY Patent Application

SEARCHED	INDEXED
SERIALIZED	FILED

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/943,184		365	251	315	2818

APPLICANTS  
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TITLE  
Programmable array logic or memory devices with asymmetrical tunnel barriers

PTO-2040  
12/89

ISSUING CLASSIFICATION					
ORIGINAL		CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
257	314	257	315	239	
INTERNATIONAL CLASSIFICATION					
H01L 29/176					
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket					

<input type="checkbox"/> TERMINAL <input type="checkbox"/> DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims 23
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____	18	27	2	Print Claim for O.G. 1
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	T6-T6 H0 02/04 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 2-13-04
 David Neils Supervisory Patent Examiner Technology Center 2800 (Primary Examiner) 2/04 (Legal Instruments Examiner) (Date)			ISSUE FEE	
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